

# Power Results at 4 GHz of AlGaIn/GaN HEMTs on High Resistive Silicon (111) Substrate

N. Vellas, C. Gaquière, A. Minko, V. Hoël, J. C. De Jaeger, Y. Cordier, and F. Semond

**Abstract**—The high potential at microwave frequencies of AlGaIn/GaN high electron mobility transistors (HEMTs) on high resistive silicon (111) substrate for power applications has been demonstrated in this letter. For the first time, an output power density close to 1.8 W/mm and an associated power added efficiency of 32% have been measured on a  $2 \times 50 \times 0.5 \mu\text{m}^2$  HEMT with a linear power gain of 16 dB. These results constitute the state of the art.

**Index Terms**—AlGaIn/GaN, high resistive silicon (111) substrate, load impedance, microwave power, pulsed measurement, traps effects.

## I. INTRODUCTION

AlGaIn/GaN high electron mobility transistors (HEMTs) have recently received considerable attention for power applications at microwave frequencies. In fact, the GaN material presents a wide band gap, a high saturation velocity, and a high thermal stability, so it constitutes an ideal candidate for such applications. At the present time, silicon carbide (SiC) and sapphire materials are the main substrates used for the GaN HEMT device production. Recently, a power density of about 10.7 W/mm has been obtained with AlGaIn/GaN HEMTs on silicon carbide at 10 GHz and 6.6 W/mm at 20 GHz [1], [2]. Nowadays, these results constitute the state of the art on silicon carbide substrate. On the other hand, the results obtained on sapphire substrate are lower. The state of the art is about 6.5 W/mm at 8 GHz and 3.3 W/mm at 18 GHz [3], [4]. GaN HEMT devices on Si substrates can be an interesting alternative because of the low cost, large area availability, and acceptable thermal conductivity (one half the thermal conductivity of SiC), and they allow the potential integration of power electronics on an advanced Si technology. Due to the higher lattice and thermal expansion coefficient mismatches, which produce a higher dislocation density and a possible generation of crack, the growth of GaN on silicon is more difficult than on sapphire and SiC substrates. An output power density of 0.55 W/mm has already been obtained on a device grown on Si substrate with  $0.3 \mu\text{m}$  gate length at 4 GHz associated with a cut-off frequency of 25 GHz and an  $f_{\text{max}}/f_t$  ratio close to the unity [5].

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N. Vellas, C. Gaquière, A. Minko, V. Hoël, and J. C. De Jaeger are with the Tiger Common Laboratory IEMN/THALES-TRT, Département Hyperfréquences et Semiconducteurs, Institut d'Electronique et de Microélectronique du Nord, U.M.R.—C.N.R.S., Villeneuve d'Ascq Cedex, France.

Y. Cordier and F. Semond are with the CRHEA-CNRS, Sophia Antipolis, Valbonne, France.

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Source	Gate	Drain
GaN (n)		1 nm
Al <sub>0.25</sub> GaN <sub>0.75</sub> (nid)		30 nm
GaN		2 $\mu\text{m}$
{AlN/GaN} sequences		0.5 $\mu\text{m}$
AlN	nucleation	50 nm
Si(111) High resistivity $\rho : 4000\text{-}10000 \Omega\cdot\text{cm}$		

Fig. 1. AlGaIn/GaN structure of HEMTs on high resistive silicon (111) substrate.

In this letter, we report small and large-signal results of AlGaIn/GaN HEMTs on a high resistive Si (111) substrate.

First, a brief description of GaN HEMT fabrication is presented. The main dc and small signal microwave results are summarized. Second, the static results are compared to those obtained by pulsed measurements and trap effects are shown. Then, the large signal characterization is described, including measurement conditions and power results obtained.

## II. DEVICE DESCRIPTION AND SMALL SIGNAL MICROWAVE RESULTS

The AlGaIn/GaN/Si structure (Fig. 1) has been grown on a high resistive silicon (111) substrate in a reactive molecular beam epitaxy system using ammoniac as the nitrogen source (Riber compact 21). More details about the layer growth can be found elsewhere [6]. The aluminum content in the AlGaIn layer is 25% with a  $300\text{-}\text{\AA}$  thickness. The devices have gate-drain and gate-source spacings of  $2 \mu\text{m}$ , a gate width of  $100 \mu\text{m}$ , and a gate length of  $0.5 \mu\text{m}$ . The ohmic contact metallization is Ti/Al/Ni/Au with respective thickness of  $150/2200/400/500 \text{\AA}$ . This contact is annealed under nitrogen atmosphere at  $900^\circ\text{C}$  during 30s. The mesa isolation is made by reactive ion etching (RIE) with an etch rate of  $180 \text{\AA}/\text{min}$ . The Schottky contact metallization is Pt/Au ( $100/1000 \text{\AA}$ ) then bonding pads deposition are achieved with Ti/Au ( $1000/4000 \text{\AA}$ ) [7]. The devices are not passivated.

Table I summarizes the electron mobility, the sheet carrier concentration at  $T = 300 \text{ K}$ , the main dc, and small

TABLE I  
ELECTRON MOBILITY, SHEET CARRIER CONCENTRATION AT  $T = 300^\circ\text{K}$ ,  
MAIN DC, AND SMALL SIGNAL RESULTS OF A  $2 \times 50 \times 0.3 \mu\text{m}^2$  HEMTs ON  
HIGH RESISTIVE SILICON (111) SUBSTRATE

Device	$\mu$ ( $\text{cm}^2/\text{Vs}$ )	$n_s$ ( $\text{cm}^{-2}$ )	$I_D$ (mA/mm)	$g_{\text{ext}}$ (mS/mm)	$V_p$ (V)	$F_f$ (GHz)	$F_{\text{MAG}}$ (GHz)	$F_{\text{MAX}}$ (GHz)	$P_{\text{DC}}$ (W/mm)
	at	at	at	at	at	at	at	at	expected
	T=300°K	T=300°K	$V_{GS}=2\text{V}$	$V_{GS}=0.5\text{V}$	$V_{GS}=0.5\text{V}$	$V_{GS}=0.5\text{V}$	$V_{GS}=0.5\text{V}$	$V_{GS}=0.5\text{V}$	at $V_{DS}=30\text{V}$
			$V_{DS}=30\text{V}$	$V_{DS}=15\text{V}$	$V_{DS}=15\text{V}$	$V_{DS}=15\text{V}$	$V_{DS}=15\text{V}$	$V_{DS}=15\text{V}$	and for
									$I_{\text{DSAT}} = 0.37\text{A/mm}$
HEMT									
Silicon	1600	$8.10^{12}$	300	60	-4	18	35	38	2.2
$2 \times 50 \times 0.5 \mu\text{m}^2$									

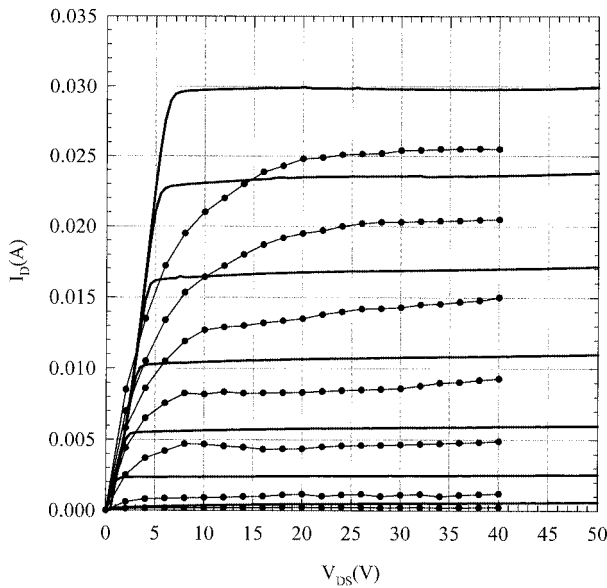


Fig. 2. Static and pulsed  $I_D(V_{DS})$  characteristics of a  $2 \times 50 \times 0.3 \mu\text{m}^2$  HEMTs on high resistive silicon (111) substrate ( $V_{GS} = -4$  to  $2\text{ V}$  step  $1\text{ V}$ ). (—) Static characteristic (---) pulsed characteristic with the quiescent bias point  $V_{GS0} = -3\text{ V}$  and  $V_{DS0} = 15\text{ V}$ .

signal microwave performance of devices with a geometry of  $2 \times 50 \times 0.5 \mu\text{m}^2$ .

The cut-off frequencies determined from the scattering parameters on a vector network analyzer (VNA) HP8510 are close to the state of the art [6]. The static and pulsed drain current characteristics versus the drain-source bias voltage for several gate-source voltages are shown Fig. 2. The pulsed  $I(V)$  measurement has been carried out at a quiescent bias point of  $V_{GS0} = -3\text{ V}$  and  $V_{DS0} = 15\text{ V}$ . This quiescent bias point (cold polarization) permits to eliminate the thermal effects and to show the traps effects. The pulsed set up is described elsewhere [8].

The static  $I_D(V_{DS})$  characteristic shows that the breakdown voltage in transistor configuration appears at a drain-source bias voltage higher than  $50\text{ V}$  at open and close channel. The drain current density is only  $300\text{ mA/mm}$  at  $V_{GS} = 2\text{ V}$ , the dc extrinsic transconductance is  $60\text{ mS/mm}$ , and the channel conductance is near zero; hence, any thermal and kink effects have been noted. The pulsed measurements opposite to static  $I(V)$  show a rise of access resistances and a decrease of the drain current. This phenomenon is attributed to the traps effects. The

low drain current density in relation to Hall effect measurements can be linked to non optimal access resistances and/or to surface effects. Effectively, a defective ohmic contact can affect the drain current performances, but the physical reasons of this phenomenon are not still explained. At present, an optimization of ohmic contacts is carrying out. The output power density expected from the static  $I_D(V_{DS})$  characteristic is  $2.2\text{ W/mm}$  ( $\Delta I \cdot \Delta V / 8$ ). This one has been calculated at  $V_{DS} = 30\text{ V}$  with  $I_{\text{DSAT}} = 370\text{ mA/mm}$  at  $V_{GS} = 3\text{ V}$ .

### III. LARGE SIGNAL CHARACTERIZATION

#### A. Setup Description and Measurement Conditions

This setup permits the device measurement at microwave frequencies on wafer or in fixture and gives the possibility to observe the power performances; the signal forms of the drain-source voltage versus biases and load impedances conditions simultaneously. It is an automatic passive load-pull system. The calibration procedures are described elsewhere [8].

A VNA allows determining the load impedance presented at the output plane of the device under test (DUT). The load impedances are carried out with a double slugs tuner.

For the measurements on wafer, the tuner cannot be placed near the output of the DUT plane. The existing loss between the tuner entry and the device output plane limits the achievable impedance values. Hence, for these components which present high breakdown voltages and low drain current densities the optimal power load impedance could not be achieved for these small total gate widths. For all that, the measurements have been done in fixture, which permits placement of the device output plane. The existing losses are strongly reduced, and almost all the impedances can be achieved.

#### B. Power Results at $4\text{ GHz}$

The power measurements have been performed near the breakdown voltage in order to obtain a high drain-source voltage swing in power condition. Thanks to the high silicon substrate resistivity, no parasitic effect linked to the substrate appears. Hence, any de-embedding is achieved.

The DUT has been biased at  $V_{GS} = 0\text{ V}$ ,  $V_{DS} = 30\text{ V}$ , and the optimal power load impedance presented at the output plane of this device is  $Z_{\text{load}}(\Omega) = 1200 + j200$ .

Fig. 3 presents the power gain, the power added efficiency (PAE), and the output power for a HEMT with a geometry of  $2 \times 50 \times 0.5 \mu\text{m}^2$  versus the absorbed input power. The maximum output power reaches  $1.8\text{ W/mm}$ , the respective power gain is about  $9\text{ dB}$  (on the other hand the linear power gain is  $16\text{ dB}$ ), and the associated PAE is  $32\%$ . Now, this power result represents the state of the art to our knowledge. The output power density expected of  $2.2\text{ W/mm}$  (see Table I) is not reached. The difference between the dc output power density expected, and the RF output power measured can be explained by the presence of traps which increase the access resistances and reduce the maximum drain-current density [9]. These effects have been checked by  $I(V)$  pulsed measurements [10]. The inferior performances of the GaN/Si devices compared to those obtained on silicon carbide or sapphire substrate might be explained by the growth technical difference. Effectively, the growth of gallium

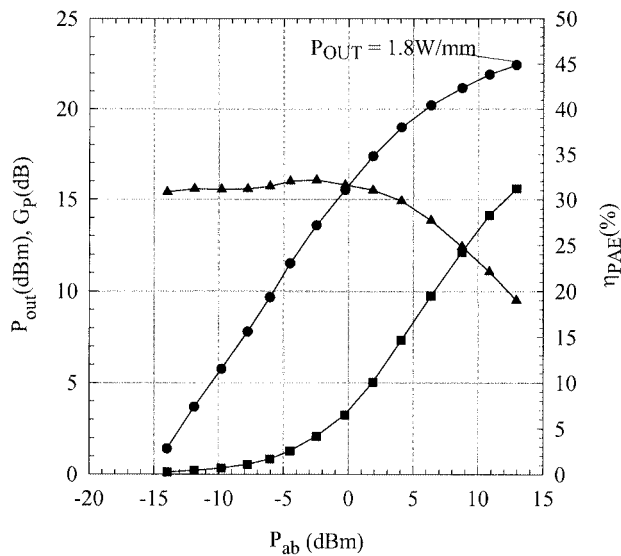


Fig. 3. RF power results at  $V_{GS} = 0$  V and  $V_{DS} = 30$  V of a  $2 \times 50 \times 0.3 \mu\text{m}^2$  HEMTs on high resistive silicon (111) substrate at 4 GHz. ( $\blacktriangle$ ) Power gain; ( $\blacksquare$ ) power added efficiency; ( $\bullet$ ) output power

nitride on silicon substrate has been achieved by MBE when in most of case the growth on the other substrate (SiC and sapphire) is achieved by metal organic chemical vapor deposition (MOCVD). Moreover, this GaN layer growth on Si substrate is less mature compared to the other one. Hence, an important improvement of microwave performances could be expected with the epitaxy and process maturity.

#### IV. CONCLUSION

An output power density of 1.8 W/mm and a linear power gain close to 16 dB have been measured with AlGaIn/GaN HEMTs on high resistive silicon (111) substrate at 4 GHz. These results constitute the state of the art. The high potential of AlGaIn/GaN/Si HEMT devices for power applications at microwave frequencies has been demonstrated. There is still a weak difference between the output power density expected and the measured one. This difference has been explained by pulsed measurements where trap effects have been shown. Moreover,

the epitaxial layers are not yet mature and can be improved in order to increase the drain current density and hence the output power density. A passivation step with  $\text{Si}_x\text{N}_y$  can be used on this sample in order to increase the drain current and the microwave output power [11]. When these improvements will be achieved, the silicon substrate could take place of sapphire and/or silicon carbide substrates.

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